CBCS SCHEME

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21EC42

Fourth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Digital Signal Processing

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Prove that the sampling of Fourier transform of a sequence x(n) results in N – point DFT using which both the sequence and the transform can be reconstructed. **(10 Marks)**

b. Compute the N – point DFT of $x(n) = a^n$ for $0 \le n \le N - 1$. And also find the DFT of the sequence $x(n) = 0.5n\ u(n)$; $0 \le n \le 3$. **(10 Marks)**

OR

2 a. Compute the circular convolution of the sequences and compare the results with linear convolution. (Use time domain approach).
$x(n) = \{1, 1, 1, 1, -1, -1, -1, -1\}$; $h(n) = \{0, 1, 2, 3, 4, 3, 2, 1\}$. **(10 Marks)**

b. If x(n(= {1, 2, 0, 3, -2, 4, 7, 5}, Evaluate the following :

i) x(0) ii) x(4) iii) $\sum_{k=0}^{7} x(k)$ iv) $\sum_{k=0}^{7} |x(k)|^2$.

Show that x(0) is always real. **(10 Marks)**

Module-2

3 a. State and prove the Periodicity property and Symmetry property of twiddle factor. **(05 Marks)**

b. Given $x(n) = \{1, 2, 3, 4\}$ and $h(n) = \{1, 2, 2\}$. Compute Linear convolution using circular convolution. **(05 Marks)**

c. Develop an 8 – point DIT – FFT algorithm. Draw the signal flow graph. Determine the DFT of the sequence, $x(n) = \{1, 1, 1, 1, 0, 0, 0, 0\}$. Using the signal flow graph, show all the intermediate results on the signal flow graph. **(10 Marks)**

OR

4 a. Find the response of LTI system with an impulse response $h(n) = \{3, 2, 1\}$ for the input $x(n) = \{2, +1, -1, -2, -3, 5, 6, -1, 2, 0, 2, 1\}$. Using overlap add method use 8 – point circular convolution. **(10 Marks)**

b. What do you mean by computational complexity? Compare the direct computation and FFT algorithm. In the direct computation of 256 – point DFT of x(n). How many
i) Complex multiplications ii) Complex additions iii) Real multiplications
iv) Real additions and v) Trigonometric function evaluations are required. **(10 Marks)**

Module-3

5 a. Design an FIR filter for the following desired frequency response

$$H_d(w) = \begin{cases} e^{-j3w} & \text{if } |w| \le \pi/4 \\ 0 & \text{if } |w| > \pi/4 \end{cases}$$

Use the Hanning window function. Obtain the frequency response of the designed FIR filter. **(10 Marks)**

b. A FIR filter is given by $y(n) = x(n) + \frac{2}{5}x(n-1) + \frac{3}{4}x(n-2) + \frac{1}{3}x(n-3)$.

Draw the lattice structure and direct form. **(10 Marks)**

OR

6 a. Design a low pass digital filter to be used in an A/D – H(2) – D/A structure that will have a -3 dB cutoff at 30 π rad/sec and an attenuation of 50dB at 45 π rad/sec. The filter is required to have a linear phase and the system will use a sampling rate of 100 samples 1 second. **(10 Marks)**

b. Given $H(z) = (1 + 0.6z^{-1})^5$. i) Realize in direct form ii) Realize as a cascade of first order sections only iii) As a cascade of 1st and 2nd order sections. **(10 Marks)**

Module-4

7 a. Derive an expression for order and cut off frequency of the Butterworth filter. **(10 Marks)**

b. Realize the following difference equation using digital structures :

i) Direct form – I ii) Direct form – II

$y(n) - \frac{3}{4}y(n-1) + \frac{1}{8}y(n-2) = x(n) + \frac{1}{3}x(n-1)$. **(10 Marks)**

OR

8 a. The system function of the analog filter is given as $H_a(S) = \frac{S+0.1}{(S+0.1)^2+16}$. Obtain the system function of the digital filter using bilinear transformation which is resonant at $w_r = \pi/2$. **(10 Marks)**

b. Realize the following system functions

$H(z) = \frac{8z^3 - 4z^2 + 11z - 2}{(z-0.25)(z^2 - 2 + 0.5)}$. Using direct form – II. **(05 Marks)**

c. List the characteristics of commonly using Analog filters. **(05 Marks)**

Module-5

9 a. Explain the digital signal processors based on Harvard architecture. **(10 Marks)**

b. Discuss briefly the following special digital signal processor hardware units :

i) Multiplier and Accumulator (μAC0 unit ii) Shifters iii) Address Generators. **(10 Marks)**

OR

10 a. Explain Fixed – Point digital signal process using basic architecture of TMS320C54X family. **(10 Marks)**

b. Illustrate the operation of circular buffers used for address generation in DS processors. **(10 Marks)**

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